



ROHDE & SCHWARZ

SERVICE INSTRUCTIONS

Transfer Memory Module CM-Z1

803.7510.02

Printed in West Germany

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1. The first part of the report is a summary of the work done during the last year. It includes a list of the main results and a brief description of the methods used.

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2. The second part of the report is a detailed description of the work done during the last year. It includes a list of the main results and a brief description of the methods used.

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3. The third part of the report is a summary of the work done during the last year. It includes a list of the main results and a brief description of the methods used.

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5.1 Function Description

This module is used to record and reproduce programmed instrument settings and data. The entered data are retained by a built-in battery supply, even if the module is not connected to the instrument, and can be read out again on the instrument or overwritten at any time.

The module can be divided into the following function units (see Fig. 5-1):

- Interface to instrument
- RAM
- Internal interface
- BUSY display
- Battery supply

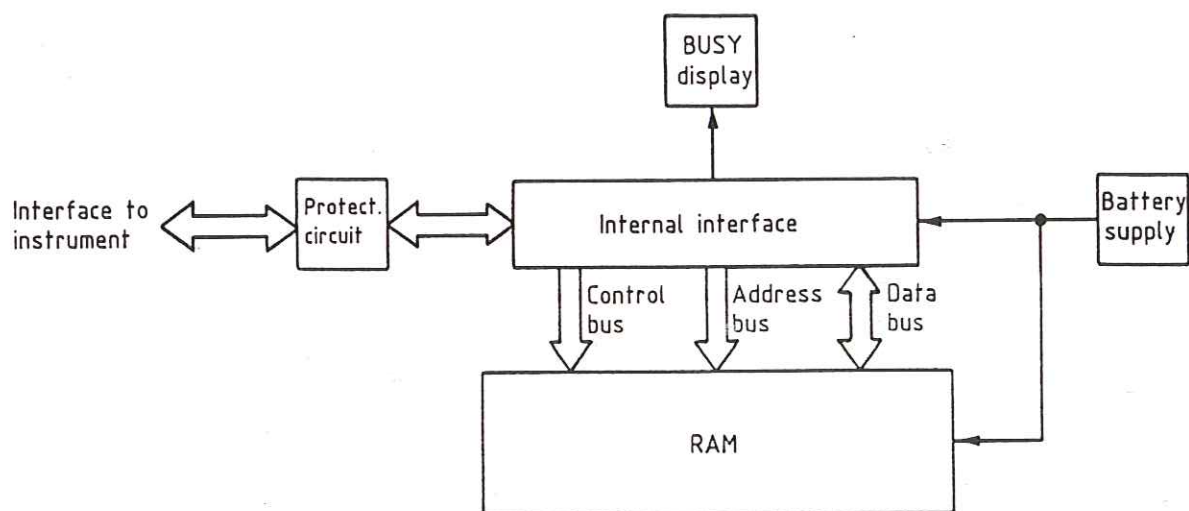


Fig. 5-1 Block diagram of the transfer memory

5.1.1 Interface to Instrument

The 9-line serial interface is used for feeding power to the module when the CMT is in operation and contains a clock line, a data line and a control line for each data direction and a line via which the battery voltage of the transfer memory can be checked at high impedance by the instrument.

5.1.2 RAM

The memory is a single 8K x 8-bit static CMOS-RAM. It is only activated via the internal interface and has no direct connection to the interface to the instrument. The built-in battery provides the power required to retain the data if power cannot be obtained from the instrument.

5.1.3 Internal Interface

This interface converts the serial data and commands from the instrument into parallel mode for the RAM and the display. The RAM data read in parallel are also transmitted to the instrument in serial mode.

a) Data direction: instrument → transfer memory

Data transfer takes place in serial mode.
The following signals are used:

CPS-L Clock line
DO-L Data line
STREM Strobe line

A complete cycle transmits 3 x 24 bits as in Fig. 5-2.

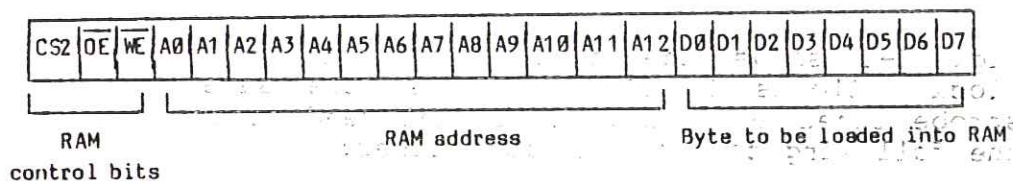


Fig. 5-2 Data flow when loading the transfer memory with one byte

D7 is transmitted first and CS2 last by the instrument. The RAM control bits contain the respective command such as write, read, disable or standby. The data flow shown in Fig. 5-2 is transmitted three times, only the contents of the RAM control bits being varied. In the first data flow, the RAM control bits are set to "Disable", in the second data flow to "Write" and in the third data flow to "Disable" again. The addresses and data remain the same. The result of this procedure is that the addresses and the data are stable in the RAM in the changeover phase from "Disable" → "Write" and "Write" → "Disable".

b) Data direction: transfer memory → instrument

Data transmission again takes place in serial mode. In this case a transfer memory read cycle comprises 3 x 16-bit data transmission in the direction from instrument to transfer memory and 1 x 8-bit data transmission from the transfer memory to the instrument.

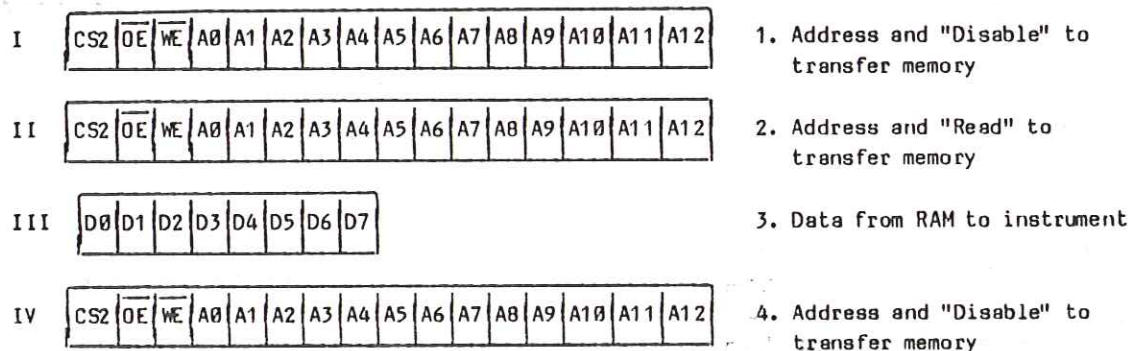


Fig. 5-3 Configuration of a transfer memory read cycle

Fig. 5-3 shows the timing and the sequence of the four blocks. Blocks I, II and IV use the same clock, data and strobe lines as in a). The actual read block (block III) uses the following control and data lines:

PSEM	Transfer pulse
CPS-L	Clock line
DATIEM	Data line

The reason for the transfer from blocks I to II and III to IV is that the address must be stable in the RAM when the change from "Disable" to "Read" or from "Read" to "Disable" takes place. The contents from A0 to A12 do not change within a cycle. A12 appears first on the data line and CS2 last. With block III, D7 appears first on the data line and D0 last.

5.1.4 BUSY Display

The BUSY display visibly indicates a read or write access to the transfer memory. Since the signal STREM is activated at least once with every read and write process, this signal can be used to drive an LED stage. The short intervals between two STREM pulses prevent the BUSY LED from flickering.

5.1.5 Battery Supply

The RAM is powered by a built-in back-up battery if the instrument power is missing. In addition, the section of the internal interface circuit which provides the control signals ($\overline{WE}$, $\overline{OE}$, CS2) for the RAM is also connected to the back-up supply. The RAM remains in the low power "Data hold" mode if CS2 = 0.

5.2 Testing and Adjustment

The module need not be adjusted. All tests should be carried out using Section 3.

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