



ROHDE & SCHWARZ

SERVICE INSTRUCTIONS

Duplex Modulation Meter Option CM-B9

803.5317.02

5	<u>Service Manual for Duplex Modulation Meter</u>	
	<u>Option CM-B9</u>	5.1
5.1	Function Description	5.1
5.1.1	Output Frequency	5.1
5.1.2	VCXO Loop	5.1
5.1.2.1	Programmable Divider by N	5.2
5.1.2.2	Fractional Divider	5.3
5.1.3	RF Loop	5.3
5.1.4	Oktave Divider	5.4
5.1.5	Control and Diagnosis	5.4
5.2	Testing and Adjustment	5.6
5.2.1	Frequency Adjustment of RF Oscillators	5.6
5.2.2	Level Adjustment of RF Oscillators	5.6
5.2.3	Testing the RF Loop	5.7
5.2.4	Testing the Spurious FM	5.7
5.2.5	Testing the Frequency Dividers	5.7
5.2.6	Testing the VCXO Loop	5.8
5.3	Troubleshooting	5.8
5.3.1	Frequencies at the Output of the N Divider	5.8
5.3.2	DC Voltage Values	5.9
5.3.3	Signal Levels	5.9
5.3.4	Control Signals for Oktave Divider	5.10
5.3.5	Control Signals for the M Divider	5.10
5.3.6	Bit Pattern	5.11
5.4	Interfaces	5.12
	Component lists	
	Circuit diagrams	
	Component layout diagrams	

5.1 Function Description

The duplex modulation meter replaces the mixing oscillator required to convert the RF to the IF which means that the instrument is able to transmit and receive simultaneously.

The module contains a frequency synthesizer which generates frequencies in the range from 31.25 MHz to 1000 MHz. Two phase locked loops are used for frequency synthesis. The individual loops are designated RF loop and VCXO loop; the RF loop generates the coarse grid and the VCXO loop the fine grid. The two phase locked loops are synchronized to a crystal reference frequency of 100 MHz in order to stabilize the output frequency. The reference frequency must be applied to the module.

5.1.1 Output Frequency

Three oscillators generate frequencies of 500 MHz to 1000 MHz; lower frequencies are obtained by dividing. The output frequency is calculated according to the following equation:

$$F_{out} = (0.2 \times M + 2 \times \frac{M}{N}) \times \frac{1}{T} \text{ [MHz]}$$

M = Coarse divider factor	2499 to 4999
N = Fine divider factor	16666 to 50000
T = Octave divider	1, 2, 4, 8, 16

5.1.2 VCXO Loop

The VCXO loop provides the reference frequency for the coarse control loop of the RF loop. A programmable frequency divider divides the externally applied 100-MHz reference frequency to values between 2 and 6 kHz; the voltage-controlled crystal oscillator (VCXO 10.002 MHz to 10.006 MHz) is fine-tuned via a phase locked loop in this frequency range. The output signal of the VCXO is mixed with 10 MHz derived from the 100-MHz reference frequency. The filtered mixture product (2 to 6 kHz) is applied to a phase detector whose output voltage tracks the VCXO. The VCXO frequency is adjusted to the frequency of approx. 50 kHz required for the coarse control loop by dividing.

The frequency range of the VCXO loop of 50.01 to 50.03 kHz has been selected such that the range of 1 step of the coarse control loop of 200 kHz is covered. The resolution of the total system results from the maximum change in frequency of the VCXO loop with a change in the divider factor N by 1. The most unfavorable value is with M at a maximum and N at a minimum and is approx. 36 Hz. Since the ranges of the coarse control loop and the VCXO loop overlap, the divider factors M and N must be adjusted optimally before triggering in order to minimize the frequency error.

5.1.2.1 Programmable Divider by N

The fractional method and the pulse swallow method are used simultaneously in this divider. D520 is a fast ECL prescaler which can divide by 10 or 11 and is provided with a control signal (:10 or :11) by the auxiliary divider D575, D585. The signal at the output of B12 with a frequency of approx. 10 MHz is applied to a monoflop to increase the pulse width and is then divided into the following two branches:

1. The programmable synchronous divider D540 to D560
2. The auxiliary divider D575, D585

The auxiliary divider is a shift register which shifts the data applied in parallel to the input with a 10-MHz clock in serial to the prescaler once during each AF clock and thus controls the division ratio 10:1 or 11:1.

The sequence described above represents the well-known pulse swallow method with frequency division. The fractional method is also implemented using the arrangement D590, D597 and D595.

The three components form an up-counter with programmable step sizes which generates an overflow signal at 256. The counter clock is the output signal of the synchronous prescaler (D540 to 560); the step size is applied by the memory IC D592 to the input of adder D595, D590. If an overflow results (pin 9), an additional "1" is written into the shift register operating as an auxiliary divider which causes a 1:10 divider cycle to be replaced at D520 by a 1:11 cycle. An additional 100-MHz period used in this manner increases the divider ratio N by an amount <1 (fractional method). Example: $N = 200.1$ is generated by dividing 9 times in succession by 200 and then once by 201.

5.1.2.2 Fractional Divider

A resolution of approx. 36 Hz (see Section 5.1.2) is insufficient for some applications. The module can therefore be extended by a fractional divider which expands the N divider factor by up to 255/256 yielding a resolution <1 Hz. The non-harmonics resulting from the principle used are a disadvantage and lead to a deterioration in the spurious FM.

The fractional divider consists of ICs D590, D595, D97; control takes place via D592 (see also Section 5.1.2.1).

5.1.3 RF Loop

The output frequency range of 500 to 1000 MHz is generated in the RF loop. This range is divided amongst three oscillators.

Range	f in MHz	Transistor
Osc. I	500 to 655	V30
Osc. II	655 to 825	V60
Osc. III	825 to 1000	V90

The oscillating transistor (BRF96) reduces the damping of a series resonant circuit by its negative impedance at the base. The inductance of the resonant circuit is implemented using a coaxial line to keep the microphony as small as possible. A voltage-variable diode is used for tuning; the tuning voltage is applied to the cathode of the voltage-variable diode via RF inductors. The output power of the oscillator is set with the adjustable constant current of the oscillating transistor. A switching stage with two transistors driven at TTL level switches the operating voltage on for the oscillator as well as a switching diode to decouple the RF in the forward direction.

The M divider is a programmable high-frequency divider with a fixed prescaler (D310) as well as a switchable prescaler (D315). The first prescaler (D310) divides the oscillator frequency by 4 down to 125 to 250 MHz. The second prescaler (D315) with the internal switchover 11/10 operates together with the so-called auxiliary counter (D330) as a decadic counter stage in the 4-digit M divider.

The prescaler 11/10 starts with a divider ratio 11:1. After 11 input pulses, the counters (D330 and D331) are simultaneously incremented by 1. If the 9 has been reached on the auxiliary counter (D330) this switches the prescaler (D315) to a divider ratio 10:1. The pulses divided by 10:1 are then only recorded by the main counter (D331, D332, D333). If these have also reached the 9, the prescaler is again set to 11:1 by a reset pulse and the other dividers to the entered divider ratio. A new counting cycle can then begin.

For example, if the divider factor is 2654, the auxiliary counter and the main counter count 4 pulses before the prescaler is switched from 11 to 10. The prescaler divides the input frequency by 10 for the remaining divider factor of the main counter (= 261). The input frequency must deliver $4 \times 11 + (256-4) \times 10 = 2564$ pulses for the complete counting cycle, which corresponds to the above dividing factor.

The M divider must be loaded with the difference between the final counter value and the divider factor because it is an up-counter. An additional 10 input pulses are used because the loading of the counters uses one clock pulse and the prescaler is set to the dividing factor 10 during this time. For example, if the divider ratio M is to be 2654, $(10009 - 2654) = 7355$ must be loaded into the counter. This value is stored in the shift registers (D360 and D365) in BCD code.

The output signal of approx. 50 kHz from the M divider is applied to the phase detector; the signal is then compared with the frequency from the VCXO loop and controls the oscillators via the subsequent integrator.

5.1.4 Octave Divider

The actual RF synthesizer only delivers frequencies in the range from 500 to 1000 MHz; lower frequencies must therefore be generated by dividing. The output signal of the oscillators is applied to the dividers via a buffer amplifier (N130). The octave divider consists of a 2:1 divider and three 4:1 dividers. These are connected such that divider ratios of 2, 4, 8 and 16 are produced. The output signals of the individual dividers are applied to the output amplifier via switching diodes.

Since the duplex modulation meter can only control the LO input of the mixer, filtering of the harmonics produced by dividing can be omitted. Subharmonics of the LO frequency may lead to undesirable non-harmonics, however, and all unrequired frequency dividers are therefore switched off.

5.1.5 Control and Diagnosis

The module is controlled via a serial data interface. The data for a complete setting (with fractionator) are stored in 8 shift registers (D360, D365, D2, D18, D550, D565, D580 and D592).

Five test points on the module can be called up by the multiplexer (D15) for diagnosis (self-test). The tuning voltages of the oscillators are also constantly monitored by window discriminators (N240, N440 and N660) and the loop OK line is set to LOW if the limits are violated.

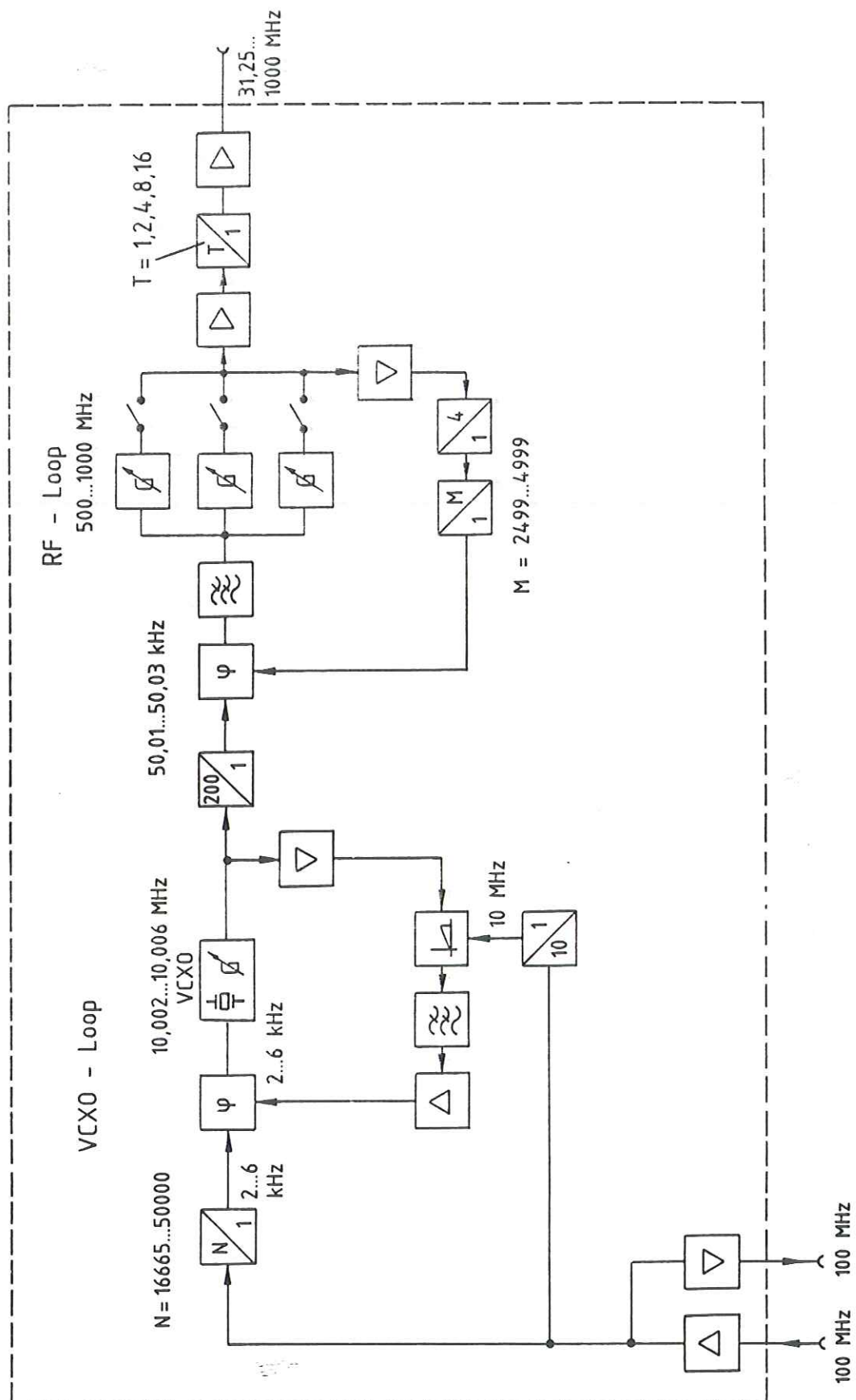


Fig. 5-1 Block diagram of the Duplex Modulation Meter

5.2 Testing and Adjustment

5.2.1 Frequency Adjustment of RF Oscillators

- Apply DC voltage of $2.5 \text{ V} \pm 0.1 \text{ V}$ to X9/2.
- Connect an RF analyzer or frequency counter to X309.
- Adjust the frequency using trimmers C21, C51 and C81 according to the following table:

Instrument setting	Frequency at X309	Trimmer
520 MHz	$500 \text{ MHz} \pm 5 \text{ MHz}$	C21
700 MHz	$655 \text{ MHz} \pm 5 \text{ MHz}$	C51
900 MHz	$825 \text{ MHz} \pm 5 \text{ MHz}$	C81

- Insert plug-in jumper X9, screw on cover. The control voltage can be measured through the hole provided in the RF shielding; the correct value should be $2.5 \text{ V} \pm 0.1 \text{ V}$ for the following frequencies:

Frequency at X309	Trimmer
500 MHz	C21
655 MHz	C51
825 MHz	C81

5.2.2 Level Adjustment of RF Oscillators

- Apply DC voltage of $12 \text{ V} \pm 0.5 \text{ V}$ to X9/2.
- Connect RF analyzer to X309.
- Ensure that no subharmonics occur. They are influenced by R49, R79, R109.
- Adjust the frequency using trimmers R49, R79 and R109 according to the following table:

Instrument setting	Level at X309	Trimmer
520 MHz	$-3 \text{ dBm} \pm 3 \text{ dB}$	R49
700 MHz	$-3 \text{ dBm} \pm 3 \text{ dB}$	R79
900 MHz	$-3 \text{ dBm} \pm 3 \text{ dB}$	R109

5.2.3 Testing the RF Loop

- Connect a frequency counter and a power meter to the RF terminator X309. Check the level and frequency with the following instrument settings.
- Frequency setting on instrument:
 - 501 MHz
 - 654 MHz
 - 656 MHz
 - 824 MHz
 - 826 MHz
 - 1000 MHz
- The frequency must agree with the setting.
- The level must be $-3 \text{ dBm} \pm 3 \text{ dB}$.
- The tuning voltage at X9/1 must be in the range 2.5 V to 20 V.

5.2.4 Testing the Spurious FM

The spurious FM must be tested with the module closed.

- Connect modulation analyzer to X309.
- Adjust frequencies on the instrument in the range from 500 to 1000 MHz and measure the spurious FM.
- The spurious FM (weighted to CCITT, RMS) must be $< 12 \text{ Hz}$.

5.2.5 Testing the Frequency Dividers

- Connect DC voltage source (2 V to 20 V) to X9/2.
- Connect RF analyzer to X309.
- Set the following frequencies on the instrument and sweep the complete voltage range in each case.
 - f in MHz: 900, 700, 520, 450, 350, 260, 225, 175, 130, 113,
87, 65, 57, 44, 32.
- Check on the analyzer that no non-harmonics or subharmonics occur.
- The level must be $-3 \text{ dBm} \pm 3 \text{ dB}$ in the complete frequency range (approx. 30 MHz to 1000 MHz).

5.2.6 Testing the VCXO Loop

a) Instrument setting: frequency 500.1 MHz

- The tuning voltage at X6 must be >3 V.
- The frequency at X3 must be 10.002 MHz.

b) Instrument setting: frequency 500.3 MHz

- The tuning voltage at X6 must be <12 V.
- The frequency at X3 must be 10.006 MHz.

5.3 Troubleshooting

Troubleshooting can be readily carried out using the specified DC voltage values and signal levels. The inductors L30, L60 and L90 should be checked if the RF oscillators have a high microphony sensitivity. The inductors must be adhered firmly onto the circuit board.

5.3.1 Frequencies at the Output of the N Divider

The frequency of the N divider should be tested at P1 in the case of small frequency errors (<200 kHz).

a) Determination of M divider factor:

$$M = \text{INT} \left(\frac{F_{\text{OUT}}}{50.01} \cdot 250 \right) [\text{MHz}]$$

b) Determination of N divider factor:

$$N = 2xM / (F_{\text{OUT}} - 0.2xM) [\text{MHz}]$$

c) Determination of frequency at P1: $F_{P1} = 100 \text{ MHz}/N$

5.3.2 DC Voltage Values

Emitter V30, V60, V90	-9 V $\pm$ 1.5 V
X6	3 to 12 V
X9	2.5 to 20 V
P12	12 V $\pm$ 1 V
P11	-11 V $\pm$ 1,5 V
D140/6 (switched off)	<0.5 V
D160, D170, D180/2 (switched off)	<0.5 V
N400/3	2.5 V $\pm$ 0.3 V
D260/6	8.6 V $\pm$ 1 V
Emitter V230	6.8 V $\pm$ 1 V

5.3.3 Signal Levels

N500/4	100 MHz	ECL
D510/5	10 MHz	ECL
P5	approx. 10 MHz	ECL
P6	approx. 10 MHz	TTL
D570/12	100.02 to 100.06 kHz	TTL
P1	2 to 6 kHz	TTL
P2	2 to 6 kHz	TTL
X3	10.002 to 10.006 MHz	approx. 4 V _{pp}
N260/3	2 to 6 kHz	50 to 150 mV _{pp}
X8	approx. 50 kHz	TTL
P3	approx. 50 kHz	TTL

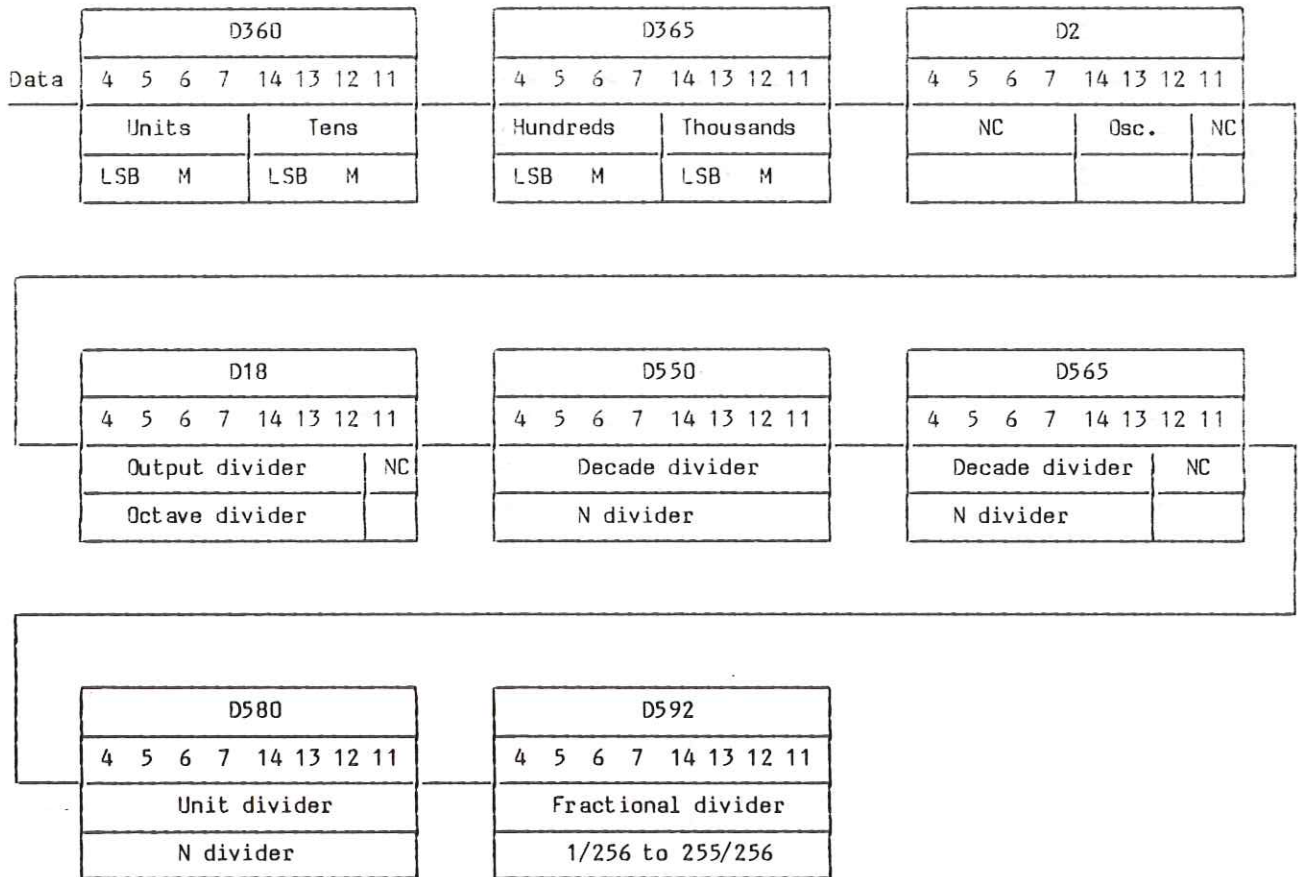
5.3.4 Control Signals for Octave Divider

Frequency at X309 in MHz	Control signals at D18						
	Pin						
	4	5	6	7	14	13	12
500 to 1000	0	1	1	1	1	0	0
250 to 500	1	0	1	1	1	1	0
125 to 250	1	1	0	1	1	0	1
62.5 to 125	1	1	1	0	1	1	0
31.25 to 62.5	1	1	1	1	0	0	1

5.3.5 Control Signals for the M Divider

Frequency at X309 in MHz	Control signals															
	D365								D360							
	Pin															
	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4
802	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1
801.8	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0
801.6	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0
801.2	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0
800.4	0	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0
800	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0
798	0	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0
794	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0
786	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
782	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0
762	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0
722	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0
642	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0
842	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0

5.3.6 Bit Pattern



5.4 Interfaces

Coaxial Interfaces

Pin	Frequency	Level
X931	100 MHz (input)	-3 dBm $\pm$ 3 dB
X932	100 MHz (output)	800 mV _{pp} , ECL
X939	31.25 to 1000 MHz	-3 dBm $\pm$ 3dB

Multipoint connector X1:

A12, A13, B12, B13	+5-V power supply
A15, B15	+24-V power supply
A17, B17	+15-V power supply
A19, B19	-15-V power supply
A2, B2	Ground
A7, B7	
A9, B9	
A11, B11	
A14, B14	
A16, B16	
A18, B18	
A20, B20	
A30, B30	
A32, A32	
A10, B10	Clock
A8	DATA
A6	STROBE
B21	Data programming
A23	Test voltages