



ROHDE & SCHWARZ

SERVICE INSTRUCTIONS

Display/Keyboard Module

802.3662.00

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5.1 Function Description

The display/keyboard module consists of five units:

- Key detection
- Rotary pulse generator (spinwheel)
- Display control
- LED/illumination control
- Loudspeaker amplifier

5.1.1 Key Detection

All keys on the front panel (except the STANDBY key) are combined into a matrix.

In the reset state, the columns (KQ0 to KQ9) are held Low (static) by a port of the main controller, the flip-flop D7.I being reset by a pulse on line RESKFF (active High).

The signal REPEAT (active High) is produced by ANDing (D6) when any key is pressed and leads to an interrupt of the main controller on the digital unit module (KEYINT, active High, edge-triggered). The number of the pressed key is determined by the software as follows:

- a) All column inputs KQ1 to KQ9 to High, KQ0 to Low.
If one of the row outputs KA0 to KA7 is Low, the pressed key is at position KQ0/KAx ($0 \leq x \leq 7$).
- b) Repetition of a).
For all columns (KQ1 to KQ9 in succession to Low).
- c) The value is only processed further if unequivocal pressing of a key has been detected; the interrupt is otherwise ignored (contact bounce or simultaneous pressing of several keys).
- d) The keyboard is activated again following key detection, i.e. all columns are set to Low and the flip-flop is reset.

Key debouncing is also handled by the software, i.e. the key detection routine only starts 20 ms after the interrupt has been generated (switch-on bounce) and resetting of flip-flop D7.I 20 ms after the signal REPEAT has dropped out (switch-off bounce).

5.1.2 Rotary Pulse Generator

The rotary pulse generator is a magnetic disk with 12 north and south poles, two permanent magnets for latching in and two Hall generators with associated logic to detect movements and directions (24 pulses per rotation).

When the spinwheel is rotated, two squarewave signals with a mark-to-space ratio of 1:1 are present at test points P6 and P7 offset in phase by 90 degrees. Each rising and falling edge at P7 generates an interrupt for the controller via D4.IV, D3.I, D3.II, D2.III, D4.I and D4.II (DREINT, active High, edge-triggered) provided that flip-flops D3.I and D3.II have been reset by pulse DRERES (active Low). The direction information provided by D1.I, D1.II, D2.I and D2.II is transferred by the reset pulse (DRERES) to flip-flop D5.I and is available at connection DREDIR (High corresponds to clockwise).

Evaluation sequence:

1. Reset rotary pulse generator (Low pulse at DRERES).
2. Second reset following interrupt by DREINT (High) + direction information available at DREDIR. Buffer counter (software) is incremented or decremented by main controller.
3. DREINT is enabled on the digital unit module.

5.1.3 Display Control

The LCDs are driven in multiplex mode by special drivers (D10 to D18). The multiplex depth is 4 (backplanes), the multiplex frequency approx. 200 Hz.

The drivers are in the basic status following the switch-on reset (>100 ms !) at connection RESET (active High), i.e. all LCD segments are dark. The drivers must first be initialized (COMMAND mode, LCDCD High) via the lines LCDSI (data, active High), LCDCK (clock, active Low) and LCDCD (command/data switchover). The internal memory of the drivers is then loaded with the contents of the display via the same lines (now in DATA mode) in the form of a 16-byte string. The line OPTPOL is used to synchronize the slower drivers with the main controller, i.e. this line becomes High following each byte and stops the processor until the data have been processed.

The individual drivers are selected by the shift registers D20 and D21 via the serial channel LCD-SEL (strobe) in conjunction with DO-L and CPS-L (data/clock).

All drivers are provided with a system clock of approx. 100 kHz (P5) from D18 via buffer D26.II/D26.III.

The display contrast depends on voltage V11 which is generated by V1/N1.I.

5.1.4 LED/Illumination Control

All LEDs (except the STANDBY LED) are controlled by shift registers D22, D23 and D24 via the serial channel LED (strobe) in conjunction with DO-L (data) and CPS-L (clock). Since LEDs of different luminosity are used, an additional driver (D25) is required for the green LEDs. The display illumination is controlled via a buffer (V2) and a delay element (R30/C30) in order to compensate for the PTC effect of the lamps.

5.1.5 Loudspeaker Amplifier

The AF to be amplified is coupled to X11.A8 at low impedance (impedance $\rightarrow 0 \Omega$). The control circuit for N100.I is on the analog unit and is identical to the control of N100.II. The lamps are used at this point for dynamic compression because of their PTC effect. The complementary output stages V100/V101 or V104/V105 enable the high output currents which are required because of the low circuit impedance.

5.2 Testing and Adjustment

5.2.1 Key Detection

Test: 1. Apply Low to KQ0 to KQ9.

2. The line REPEAT must become High when each key is pressed. If not: key faulty.
3. After resetting the flip-flop D7.I (pulse >500 ns at connection RESKFF, active High), a High must be present at connection KEYINT following pressing of any key until the next reset. If not: D7.I faulty (or control lines).

Adjustment: none

5.2.2 Rotary Pulse Generator

Test: When moving the spinwheel, a squarewave voltage with a mark-to-space ratio of 1:1 and a frequency 12 x rpm/3600 Hz must be measured at test points P6 and P7 with a phase offset of 90 degrees. Deviations from TTL level at test points P6 and P7 indicate a fault in the Hall generator B1 or B2. The Hall generators are maladjusted if the phase offset varies greatly from 90 degrees.

After resetting flip-flops D3.I and D3.II (Low pulse at input DRERES >500 ns, TTL level), the interrupt output DREINT must assume a High level each time the spinwheel is moved and the direction of rotation (High with clockwise rotation) following reset of output DREDIR.

Adjustment: none

5.2.3 Display Control

Test: Correct operation of the display driver largely depends on the initialization and data transmission by the controller. It is therefore recommendable to carry out the test in the instrument using the firmware test aids (e.g. D 12 SPEC) (see Section 4).

Adjust-

ment: All drivers are supplied by D18 with a system clock of approx. 100 kHz (P5) via buffer D26.II/D26.III. Potentiometer R29 can be used to compensate for component tolerances. Since the write speed directly depends on this clock, R29 is set such that flickering of the display is just no longer visible (or set to 100 kHz at P5).

The display contrast depends on voltage V11 generated by V1/N1.I. The controller R26 can be used to optimally adjust the contrast (for the respective viewing angle, generally viewed below 30 degrees from above).

5.2.4 LED/Illumination Control

Test: All LCD segments and all LEDs must light up simultaneously when the instrument is switched on.

Adjustment: none

5.2.5 Loudspeaker Amplifier

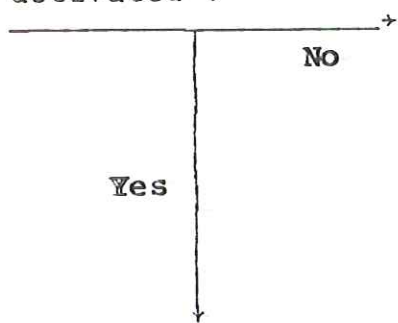
Test: Apply an AC voltage with 1 kHz/10 mV to 1 V to X11.A8 (AC coupling as result of bias of -7.5 V, internal resistance of source corresponding to lamp H 100 or 100 Ω as substitute).

Check the output signal depending on the position of the loudspeaker control and the input level using an oscilloscope or loudspeaker (AC coupling since a bias of -7.5 V!).

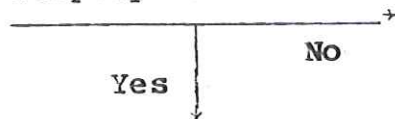
Adjustment: none

5.3 Troubleshooting

All segments
activated ?



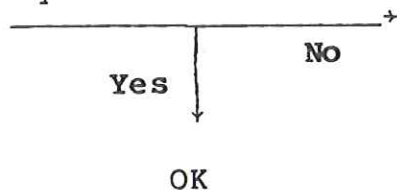
Large parts of a
display dark ?



Check solder
contacts on
LCD drivers.

Check assembly and
rubber contact of
the display.

All segments of
equal contrast ?



Check assembly and
rubber contact of
the display.