



ROHDE & SCHWARZ

SERVICE INSTRUCTIONS

RF Oscillator Module Including
Reference Oscillator Option (OCXO)
802.8835.02

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5.1 Function Description

The module contains a frequency synthesizer which delivers a frequency of 500 MHz to 1000 MHz with a resolution of 10 to 90 Hz. Two phase-locked loops are used for frequency synthesis. The individual loops are designated as RF loop and VCXO loop. The coarse spacing is generated in the RF loop and the fine spacing in the VCXO loop. The two phase-locked loops are synchronized with a crystal-stabilized reference frequency in order to obtain a stable output frequency. The output frequency is derived as follows:

$$F = (M/N) \times 400000 + M \times 200000 \text{ where } M=2499 \text{ to } 4999 \\ \text{and } N=3333 \text{ to } 10000$$

If e.g. a frequency of 750 MHz is set, then $M=3749$ and $N=7498$.

A 100-MHz crystal oscillator generates the reference source for the frequency synthesis. All frequencies generated on the module are derived from this crystal oscillator. To obtain even greater stability, this crystal oscillator can be synchronized in a phase-locked loop with an external 10-MHz reference or an oven-stabilized 10-MHz crystal (option OXCO).

5.1.1 Reference Section

The tuning diode V512 is connected in series with the crystal (B500) in the 100-MHz crystal oscillator. The frequency can be adjusted within a small range using a tuning voltage which is adjustable with trimmer R632.

The oscillator frequency divided by 10 is compared with the 10-MHz signal of the external reference or the OCXO in the digital phase detector (D610) to bring it into synchronism. The pulses generated by the phase detector are integrated by a difference integrator (N620) into a DC voltage which is applied to the voltage-variable diode V512 as a tuning voltage. The tuning voltage is controlled such that the two 10-MHz signals at the phase detector always have the same phase. Switchover from self-oscillating to synchronized operation of the 100-MHz crystal oscillator takes place automatically when using the option (OCXO).

5.1.2 VCXO Loop

The 20-MHz signal from the reference unit is converted in the amplifier (V200) from ECL to TTL level and applied to the programmable N divider.

The N divider is a decadic counter with 4 digits. The counter is incremented with each clock pulse. The preset input of the individual counters is activated via the NAND gate (D202/2) when a count of 9999 is reached and the N divider is reset by the next clock pulse. Because a clock pulse is needed for loading the counter, it counts one step more than 9999. The required divider ratio at the output of the divider is therefore 10000 minus the initial count. If e.g. the divider ratio is to be $N = 7498$, $(10000 - 7498) = 2502$ must be loaded into the counter. This value is stored in BCD in the shift registers (D205, D206). The output signal of the N divider (2 to 6 kHz) is then mixed in the subsequent phase locked mixer to 10.002 to 10.006 MHz.

The voltage-controlled crystal oscillator (VCXO) consists of the oscillating transistor V230 and the resonant circuit elements B230, V232, L230, C232 and C233. The voltage-variable diode V232 enables the frequency to be tuned in the range from 10.002 MHz to 10.006 MHz. The oscillator signal is converted into a TTL level by D250. The output of D250 pin 10 is used to drive the divider D255 (100:1). The signal is applied from pin 1 of D250 to an active mixer D262 where it is converted down with 10 MHz from the reference section. The low intermediate frequency is applied via the lowpass filter R264, C264, R265, C265 to the comparator N260 which converts the signal to TTL level for the digital phase detector.

The phase detector, consisting of D210 and D202/4, compares the phase at pins 12 and 9. The signal at pin 12 is the output frequency of the N divider. The phase detector generates positive pulses at pin 5 if the frequency at pin 9 is higher than that at pin 12. These pulses cause the tuning voltage to drop following the inverting integrator N220 in order to reestablish synchronization. If the phase-locked loop has locked, only very narrow pulses are present at pins 2 and 5 of phase detector D210.

5.1.3 RF Loop

The output frequency range from 500 to 1000 MHz is generated in the RF loop. This range is divided amongst three oscillators.

Range in MHz		Transistor
Osc. 1	500 to 655	V30
Osc. 2	655 to 825	V60
Osc. 3	825 to 1000	V90

With negative impedance at its base, the oscillating transistor reduces the damping of a series resonant circuit. The inductance of the resonant circuit is generated using a coaxial cable in order to keep the microphony as low as possible. A voltage-variable diode is used for the tuning. The tuning voltage is applied to the cathode and the FM signal to the anode of the voltage-variable diode via RF chokes. The output power of the oscillator is set by the oscillating transistor using the adjustable constant current. A switching stage with two transistors driven at TTL level switches on the operating voltage for the oscillator as well as a switching diode to decouple the RF in the forward direction. The decoupling amplifier (V158) increases the output power of the oscillators from 0 dBm to 10 dBm. Following the decoupling amplifier, the signal is applied via an attenuator pad (R160, R161) to output connector X310 and via a second pad (R164, R165) and a hybrid amplifier (N300) to the M divider.

The M divider is a programmable high-frequency divider with a fixed divider (D310) and a selectable divider (D315). D310 divides the oscillator frequency by 4 down to between 125 and 250 MHz. D315 with the internal selector 11/10 operates together with auxiliary counter (D330) as a decadic counter stage in the 4-digit M divider.

D315 commences with the divider ratio of 11:1. The counters (D330 and D331) are incremented simultaneously after 11 input pulses. Once 9 has been reached on the auxiliary counter (D330), it switches the divider (D315) to a ratio 10:1. The auxiliary counter remains at its final value. The pulses divided by 10:1 are then only counted by the main counter (D331, D332 and D333). Once the main counter has also reached 9, the divider is again set to 11:1 by a reset pulse and the other dividers are set to the entered ratio. A new counting cycle can then commence. For example, if the dividing factor is 2654, the auxiliary counter and the main counter count 4 pulses and then the divider is switched from 11 to 10. The divider divides the input frequency by 10 for the remaining factor of the main counter (=261). The input frequency must deliver $4 \times 11 + (265 - 4) \times 10 = 2654$ pulses for the complete counting cycle; this corresponds to the above dividing factor.

The M divider must be loaded with the difference between the final count and the dividing factor because it counts upwards. Ten additional input pulses are used because the loading of the counters requires 1 clock pulse and the divider is set to a factor of 10 during this period. For example, if the divider ratio is to be $M = 2654$, then $(10009 - 2654) = 7355$ must be loaded into the counter. This value is stored in BCD code in the shift registers (D360 and D365).

With FM switched off, the output signal of the M divider (approx. 50 kHz) is directly applied to the phase detector (D390) via a gate (D371). The phase detector compares this signal with the frequency of the VCXO loop divided by 200 and readjusts the RF oscillator using the subsequent integrator (N400) if there is a difference in phase. If FM is switched on, the control bandwidth should be small to enable frequency modulation with low modulation frequencies. This is achieved by switching over the integrator time constants and reducing the phase detector current. Furthermore, the input frequency of the phase detector is divided by 5 using divider (D370).

5.1.4 Control and Diagnosis

The module is controlled via a serial interface. The data for a complete setting are stored in 6 shift register ICs (D360, D365, D205, D206, D2, D18).

Eight different test points on the module can be polled by the multiplexer (D15) for diagnostic purposes. The tuning voltages of the oscillators are also constantly monitored by window discriminators (N240, N440, N660) and the loop-OK line is set to Low if the limits are violated.

5.2 Testing and Adjustment

5.2.1 Adjusting the 100-MHz Crystal Oscillator

- Plug the module onto the service adapter (included in service kit). Remove the OCXO option if fitted.
- Connect a voltmeter to anode V506. Adjust the voltage for minimum ($11.7 \text{ V} + 0.1\text{V}/-0.2 \text{ V}$) using L500.
- Connect a voltmeter to X11 (jumper X11 remains inserted) and a frequency counter to RF connector X304. Set the frequency to $100 \text{ MHz} \pm 100 \text{ Hz}$ using trimmer R632. The voltage at X11 is to be $8 \pm 1.5 \text{ V}$. Change L512 to $0.27 \mu\text{H}$ if the voltage is too high and to $0.39 \mu\text{H}$ if the voltage is too low (trimming value).
- Carry out the fine adjustment with the module closed. Adjust the frequency to $100 \text{ MHz} \pm 50 \text{ Hz}$ using trimmer R632.

5.2.2 Testing the Synchronization with an External 10-MHz Reference Frequency

- Set instrument to "External reference frequency".
- Connect frequency counter to RF connection X304.
- Apply a frequency of 10 MHz with a level of -7 dBm to connector REF 10 MHz . Operate the signal generator and the frequency counter with the same reference frequency. The output frequency at X304 must change from 99.99995 MHz to 100.0005 MHz when the input frequency changes from 9.999995 MHz to 10.005 MHz .

5.2.3 Adjusting the Reference Oscillator Option (OCXO)

- Set instrument to "Internal reference frequency".
- Wait 15 minutes for instrument to warm up.
- Connect calibrated frequency counter to X304.
- Adjust the frequency to $100 \text{ MHz} \pm 5 \text{ Hz}$ using trimmer "REF. FREQ. OPTION".

5.2.4 Testing the VCXO Loop

a) Instrument setting: frequency 500.1 MHz.

- The tuning voltage at X6 must be > 3 V.
- The frequency at X3 must be 10.002 MHz.

b) Instrument setting: frequency 500.3 MHz.

- The tuning voltage at X6 must be > 12 V.
- The frequency at X3 must be 10.006 MHz.

5.2.5 Frequency Adjustment of the RF Oscillators

- Apply a DC voltage of 2 V $\pm$ 0.1 V to X9/2 and 3.
- Connect an RF analyzer or a frequency counter to RF connection X310.
- Set trimmers R49, R79, R109 to maximum current.
- Adjust the frequency according to the following table using trimmers C21, C51 and C81:

Instrument setting	Frequency at X310	Trimmer
520 MHz	500 MHz $\pm$ 5 MHz	C21
700 MHz	655 MHz $\pm$ 5 MHz	C51
900 MHz	825 MHz $\pm$ 5 MHz	C81

5.2.6 Testing the RF Loop

- Connect a frequency counter and a power meter to RF connection X310. Check the level and the frequency with the following instrument settings.
- Frequency setting on instrument:
 - 501 MHz
 - 654 MHz
 - 656 MHz
 - 824 MHz
 - 826 MHz
 - 1000 MHz
- The frequency must agree with the setting.
- The level must be 0 dBm $\pm$ 3 dB.
- The tuning voltage at X9 must be between 2 and 20 V.

5.2.7 Testing the Spurious FM

Test the spurious FM with the module closed.

- Connect modulation analyzer to RF connection X310.
- Set various frequencies between 500 and 1000 MHz on the instrument and measure the spurious FM.
- The spurious FM (weighted to CCITT, RMS) must be < 8 Hz.

5.3 Troubleshooting

Troubleshooting can be readily carried out using the DC voltages and signal levels specified. The inductors L30, L60 and L90 must be checked if the RF oscillators have a high microphony sensitivity. The inductors must be positively adhered to the circuit board.

5.3.1 DC Voltage Values

Source V500	1.5 V $\pm$ 0.5 V
Emitter V540	2.2 V $\pm$ 0.3 V
N520/pin 11	3.8 V $\pm$ 0.5 V
N570/pin 11	3.8 V $\pm$ 0.5 V
Emitter V230	6.8 V $\pm$ 1 V
D260/pin 6	8.6 V $\pm$ 1 V
N400/pin 3	2.5 V $\pm$ 0.3 V
Emitter V30, V60, V90	-9 V $\pm$ 1.5 V
Collector V158	6.5 V $\pm$ 1 V

5.3.2 Signal Level

N520/pin 7	100 MHz	ECL
N580/pin 7	10 MHz	TTL
D202/pin 3	20 MHz	TTL
P1	2 to 6 kHz	TTL
P2	2 to 6 kHz	TTL
X3	10,002 to 10,006 MHz	approx. 4 V _{pp}
X7	10 MHz	approx. 30 mV _{pp}
N260/pin 3	2 to 6 kHz	50 to 150 mV _{pp}
X8	50 kHz	TTL
P3,P4	50 kHz (10 kHz with FM)	TTL

5.3.3 RF Level

The RF levels have been measured using a 500- Ω probe.

P5	500 to 655 MHz	-12 to -3 dBm
P6	655 to 825 MHz	-10 to 0 dBm
P7	825 to 1000 MHz	-12 to -5 dBm
P8	500 to 1000 MHz	+5 to +10 dBm
P9	500 to 1000 MHz	-4 to +5 dBm
P10	500 to 1000 MHz	-12 to -5 dBm
P11	500 to 1000 MHz	-6 to +2 dBm
P12	125 to 250 MHz	+4 to +9 dBm

5.3.4. Testing the Control Signals for the M Divider

Frequency setting on instrument (MHz)	Control signals at															
	D365								D360							
	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4
802	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
801.8	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1
801.6	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0
801.2	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0
800.4	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0
800	0	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0
798	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0
794	0	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0
786	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0
782	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0
762	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0
722	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0
642	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0
842	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0

5.3.5 Testing the Control Signals for the N Divider

Frequency setting on instrument (MHz)	Control signals at															
	D206								D205							
	11	12	13	14	7	6	5	4	11	12	13	14	7	6	5	4
500.1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
500.6002	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1
1000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
999.8	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
999.4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
999.2	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
998.2	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
996.2	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
992.2	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
990.2	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
980.2	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
960.2	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
920.2	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
900.2	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
800.2	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
600.2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

5.4 Interfaces

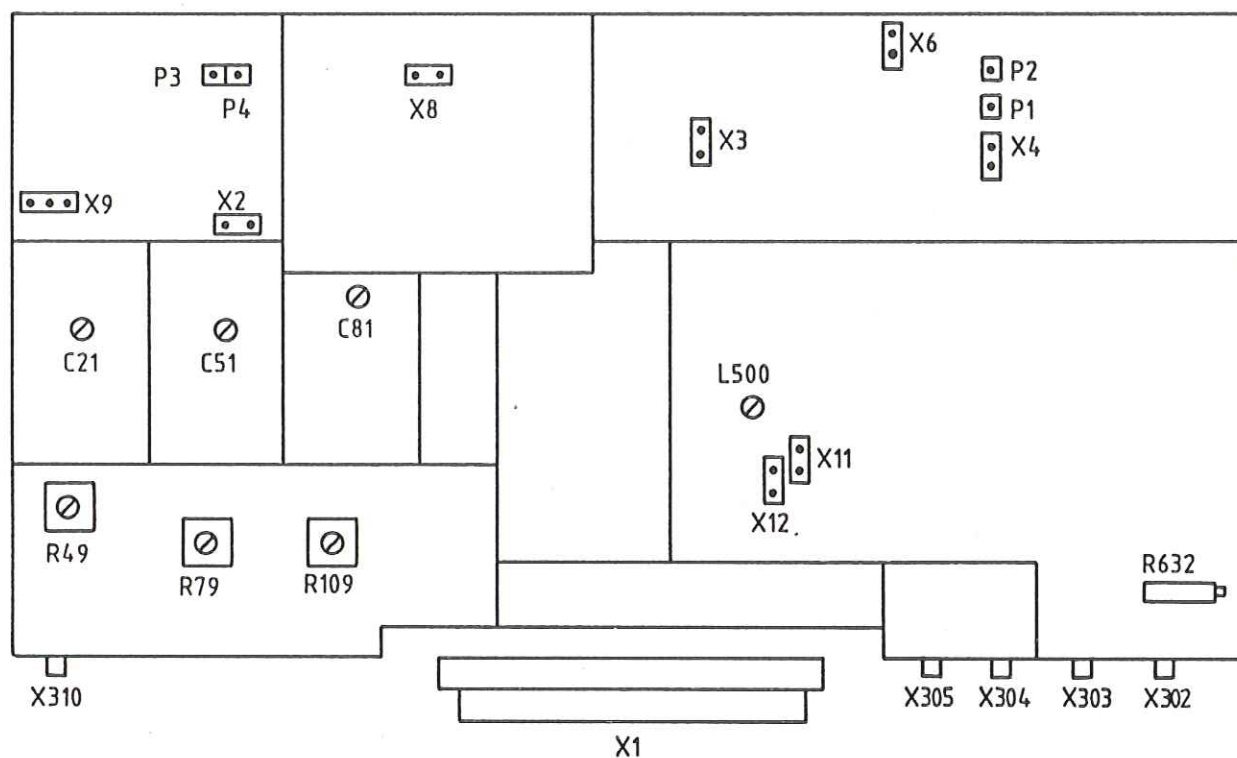


Bild 5-2 Location of the inputs/outputs and trimmers

Terminal	Designation	Frequency	Level
X302	REF.INT/EXT	10 MHz	0 dBm $\pm$ 3 dB
X303	10-MHz clock	10 MHz	TTL
X304	100-MHz ref.	100 MHz	0 dBm $\pm$ 3 dB
X305	100 MHz LO	100 MHz	0 dBm $\pm$ 3 dB
X310	RF output	500 to 1000 MHz	0 dBm $\pm$ 3 dB
X1.3	Loop OK	DC	0 to +5 V
X1.23	Test	DC	0 to +5 V
X1.31	FM input	50 Hz to 100 kHz	0 to 1 V _{rms}

Serial interface

X1.6	Strobe
X1.8	Data
X1.10	Clock