



ROHDE & SCHWARZ

SERVICE INSTRUCTIONS

Digital Unit

802.4517.02

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5.1 Function Description

The module comprises a complete processor with several special digital function groups. The processor is the central control and arithmetic unit of the instrument. It controls the complete hardware, can respond to certain peripheral events, controls simple and complex test sequences and carries out various calculations.

The digital unit contains its own 16-bit data bus and its own 20-bit address bus.

Fig. 5-1 shows the block diagram of the digital unit with the most important data and control lines where a link may consist of several signal lines.

Further units are also present on the module (RF counter, AF counter, A/D converter) whose functions are closely associated with the digital unit.

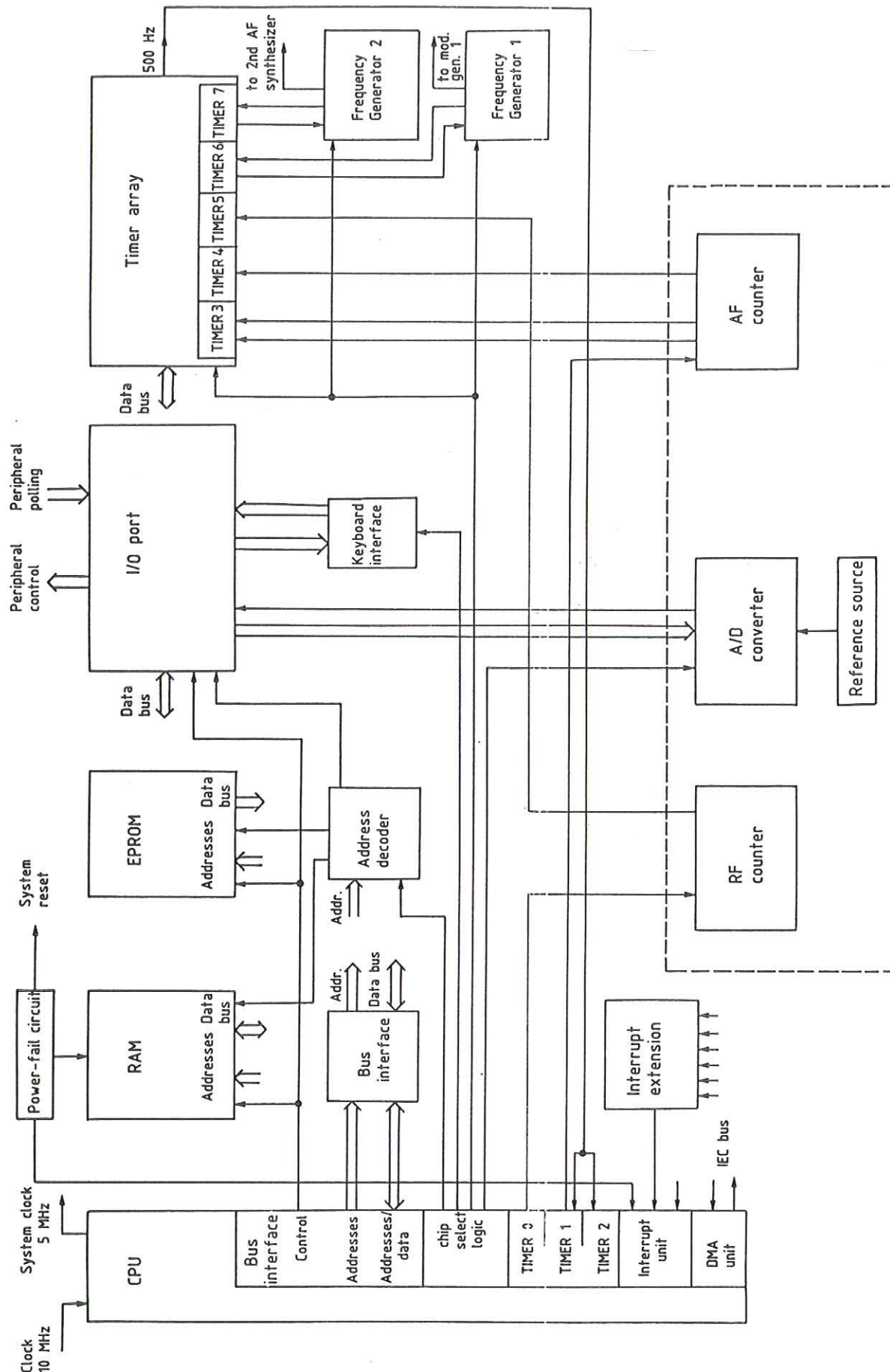


Fig. 5-1 Block diagram of the digital unit

5.1.1 CPU

A CPU of type 80186 is used. This 16-bit CPU uses an external clock of 10 MHz; the system clock is then 5 MHz.

The CPU has certain special features which are described below:

a) Bus interface

In addition to a number of control and status lines leading to and from the bus interface, this unit generates the most significant 4 address bits on special lines. The least significant 16 address bits are available on a common bus in multiplex mode with the 16 data bits. It is therefore necessary to temporarily store the least significant 16 address bits in an external bus interface (see Section 5.1.2).

b) Chip select logic

The CPU contains a chip select unit which provides various chip select outputs. This unit can be programmed such that the outputs only become active with certain address areas of the address bus.

A differentiation must be made between the memory and peripheral selection outputs. Seven selection outputs are available for driving peripheral modules. The CPU can be programmed for memory mapped or separate I/O area organization. The I/O area organization is used in this instrument. The peripheral selection outputs drive the I/O modules, the timer array, the A/D converter and the divider.

There are 6 memory selection outputs present which are not sufficient for the complete memory space of the instrument. They therefore first control, together with address lines, an external address decoder which may also be simply omitted as a result of the preselection in the CPU-internal chip select unit (see Section 5.1.3).

c) Timer unit

This unit contains 3 programmable timer/counter functions which may operate separately or as a group.

Timers 0 and 1 have external inputs and outputs. Timer 0 provides the gate time for the RF counter and timer 1 the gate time for the AF counter. These gate times can only be generated using an external reference clock of 500 MHz provided by the timer array.

Timer 2 is only used internally as the real-time clock of the system. It causes an internal interrupt every 10 ms which increments the clock.

d) Interrupt unit

The interrupt unit contains an interrupt controller with a non-maskable input (NMI) and four maskable inputs (INT0 to INT3). The NMI input is connected to the power-fail circuit. An interrupt is generated as soon as the operating voltage drops below a defined value and measures for data protection are initiated (see Section 5.1.11).

The priority of inputs INT0 to INT3 can be selected. Since their number would be insufficient for the instrument, input INT0 is expanded into six interrupt inputs using an external interrupt extension (see Section 5.1.7).

Examples of interrupt generators:
rotary pulse generator (spinwheel), keyboard, IEC bus, Centronics interface.

e) DMA unit

The DMA unit enables the fastest possible data transfer with peripheral units. This transmission mode is used together with the IEC bus.

5.1.2 Bus Interface

Since the microprocessor activates data and addresses in multiplex mode, it is necessary to store the addresses temporarily. Addresses A0 to A18 are loaded into intermediate memories. The control pulse required (ALE) is provided directly by the microprocessor.

The data bus D0 to D15 is controlled via line drivers. The CPU also provides the control signals for the data direction and activation in this case.

The address and data buses are local buses of the digital unit.

5.1.3 Address Decoder

The address decoder is responsible for selection of the various address areas of the complete memory. The input is provided by the CPU with certain address lines and lines from the chip select logic. A further signal (BHE) can be used by the CPU to trigger individual bytes from the memory with 16-bit word organization. The decoder provides single signals at the output with which the individual memory areas can be directly selected.

5.1.4 RAM

The RAM of the digital unit has a capacity of 16 Kbyte and is divided into 16x8 Kbit. Static CMOS-RAMs are used. These low power types enable battery back-up when the power supply is switched off or if it fails. For this reason, the RAM has its own power supply which is automatically switched over in the power failure circuit (see Section 5.1.11).

5.1.5 EPROM

The read-only memory has six IC sockets which can be occupied by type 27256 chips. The total memory capacity is then 192 Kbyte.

5.1.6 I/O Port

This function unit is used to trigger and scan peripheral units. The link to the microprocessor consists of the common data bus, control signals from the CPU and triggering via the address decoder. The I/O data transmission is implemented in different ways. Most of I/O lines are provided by the programmable port chips D17 and D18.

D17 is programmed as a pure output port with 25 output signals which are mainly used as strobe signals for controlling a series of peripheral shift registers. This port also provides the serial data line DO-L and the associated clock line CPS-L.

D18 is programmed to service 12 outputs and 12 inputs. The outputs also include a number of strobe lines, the serial data line DO-S and the associated clock line CPS-S. Data from peripheral modules can be read in via the inputs.

The port chips D45 and D46 represent a pure output port which provides further strobe and control lines and controls the A/D converter.

5.1.7 Interrupt Extension

It is necessary to extend the CPU-internal interrupt controller since the number of peripheral modules which require an interrupt is larger than the number of CPU interrupt inputs.

An interrupt expander with six inputs is therefore connected prior to the CPU interrupt line INT0.

Fig. 5-2 shows the block diagram of the circuit.

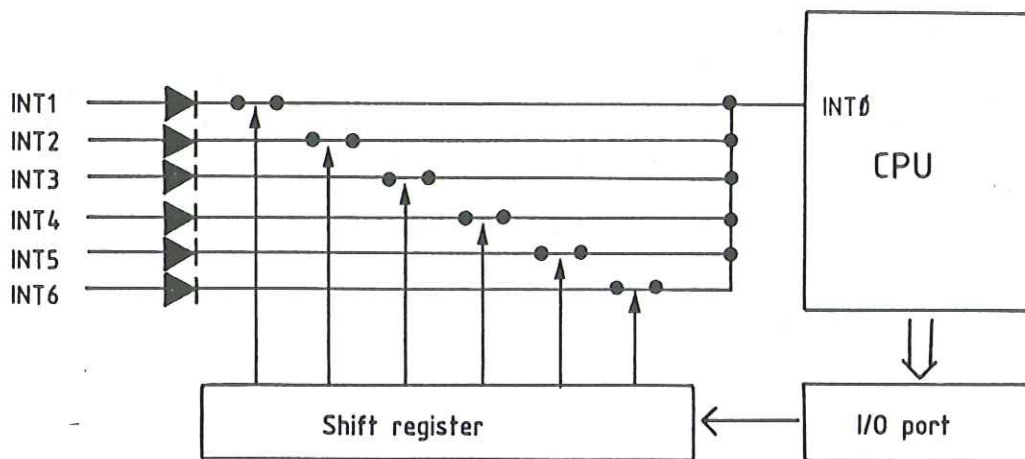


Fig. 5-2 Interrupt extension

The additional interrupt lines INT1 to INT6 are connected to a common point via a wired-OR link with serial, intermediate switches; the lines are taken to the interrupt line INT0. The switches are normally closed. If an interrupt is requested via one of the lines INT1 to INT6, the CPU starts the interrupt program and a polling sequence. A serial shift register is accessed via the I/O port which in turn accesses the interrupt switches. The interrupt program first causes all switches to open. Signal INT0 becomes inactive. The switches are then closed in sequence. The source of interrupt is identified as soon as signal INT0 at the CPU interrupt input becomes active again and the program can service the actual interrupt request.

The shift register (D33) is controlled by the I/O ports with the following signals:

CPS-S	Clock line
DO-S	Data line
HFC	Strobe line

The switches (D36, D38) are analog switches.

5.1.8 Timer Array

The timer array consists of a single chip. It contains 5 independent timers which can be programmed as clocks, counters or pulse generators. Data exchange with the CPU takes place via the common data bus, additional control lines control the chip. The timer array also provides a 500-Hz reference clock to generate the gate times in the CPU-internal timers.

Summary of assignment, use and operating modes of the timers:

Timer	Operating mode	Use
3	Counter	Evaluation of AF counter
4	Counter	Evaluation of AF counter
5	Counter	Evaluation of RF counter
6	Divider	Control of frequency generator 1
7	Divider	Control of frequency generator 2

5.1.9 Frequency Generators

Two identical frequency generator circuits are present in the digital unit whose output signal is required to generate programmable sinewave frequencies. The output signal is first extended in a monostable flip-flop and then passed on at a lower level to suppress interferences.

Each frequency generator consists of an intermediate memory, an adder, an input memory and a programmable decrementer.

Timer 6 assumes the function of the decrementer for generator 1.

Timer 7 assumes the function of the decrementer for generator 2.

The generator numbers are as follows:

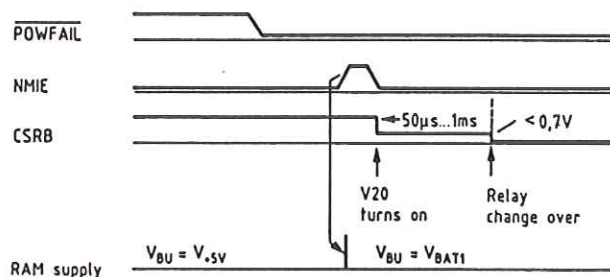
- Generator 1 (D20 to D23)
- Generator 2 (D25 to D28)

5.1.10 Keyboard Interface

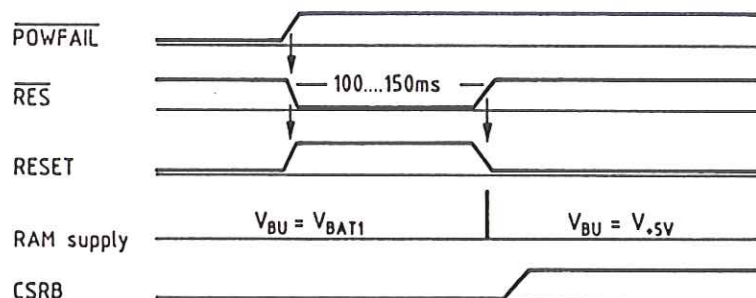
The interface comprises a 10x8 matrix with the keys located at the points of intersection. The 10 columns of the matrix are linked to an output port (D29, D30), the 8 rows to an input port (D31). Both ports are linked to the CPU via the data bus. In addition, selection lines and read or write lines lead to the two ports. A pressed key triggers an interrupt and the associated interrupt program then applies a test bit to all 10 rows in succession and polls the input port. In this manner, the point of intersection in the matrix at which a key was pressed can be determined.

5.1.11 Power-Fail Circuit

The power-fail circuit receives an active power-fail signal as soon as the monitored supply voltage drops below a critical value and then triggers an interrupt. The CPU then carries out a save routine and transmits a signal to the power-fail circuit following the last access to the RAM. The RAM supply is then switched over to the battery and the RAMs are transferred to low power mode. The power-fail signal enters the inactive status when the instrument is switched on and the critical value of the supply voltage has been exceeded. The circuit then triggers a system reset and subsequently switches over the RAM supply from the battery to the power pack. The control signal CSRB for low power mode of the RAMs is cancelled at the same time.



Sequence following transition of signal $\overline{\text{POWFAIL}}$ from High to Low.



Sequence following transition of signal $\overline{\text{POWFAIL}}$ from Low to High.

5.1.12 A/D Converter Unit

The A/D converter unit consists of the A/D converter and a reference voltage source used as the system reference (see Fig. 5-3).

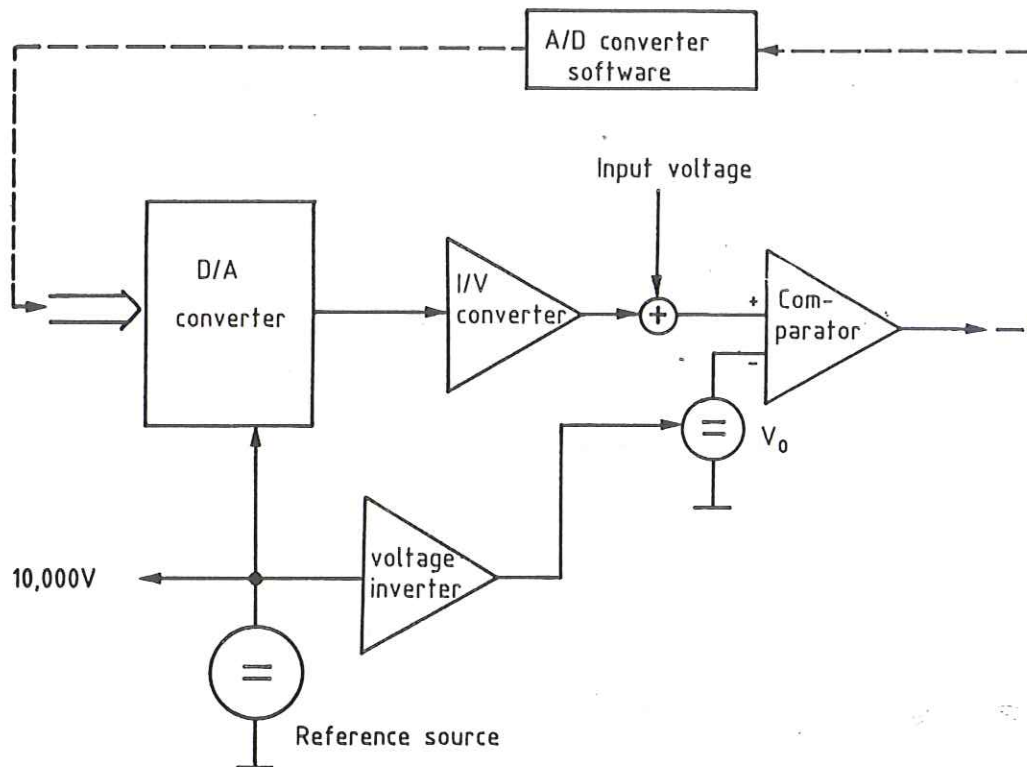


Fig. 5-3 Block diagram of the A/D converter unit

5.1.12.1 Reference Source

The reference source is designed using a temperature-compensated reference diode buffered via an operational amplifier. The voltage should be $10.000\text{ V} \pm 1\text{ mV}$ and can be set exactly using a trimmer.

5.1.12.2 A/D Converter

The A/D converter is used for digital acquisition of several analog variables and operates according to the principle of successive approximation.

Apart from the hardware, the A/D converter also contains a software program which drives the D/A converter with a 10-bit binary value during conversion of the applied input voltage. The D/A converter outputs a proportional current which is then converted into a proportional negative voltage by an inverting I/V converter. This voltage and the positive input voltage are applied to a comparator via a summation point.

If the load-independent voltage $V_O=0$ and the comparator output is High, the input voltage is higher than the voltage at the I/V converter output. This means that the D/A converter has been driven by the software with a binary value which is too small.

The program can supply the D/A converter with a more accurate binary value, however, since the software polls the comparator and has thus access to the result of the comparison. The final result is obtained after 10 such steps.

The load-independent voltage V_O at the comparator is obtained from the reference voltage and has a value of -100 mV. This enables negative voltages down to -200 mV to be detected. The upper input voltage limit of 10.2 V is above the reference voltage and is achieved by increasing the gain of the I/V converter.

5.1.13 RF Counter

(See Fig. 5-4)

The RF counter indicates the frequency of the applied RF signal in the range from 1 to 1000 MHz; the signal is first amplified, limited and then applied to a frequency divider and a transistor stage which improves the slew rate for low frequencies. The signals thus conditioned are applied via a diode switch to the divider chain consisting of a 3-bit ECL divider, an ECL/TTL converter and a 12-bit TTL divider. All dividers in the chain have binary outputs which are connected to parallel/serial shift registers which are read by the processor. The output of the divider chain is connected to a special timer chip which evaluates the divided frequency further.

A test is made whether the undivided signal or the signal divided by 4 is to be applied to the divider chain; the signal divided by 4 is first measured with a resolution of 10 kHz; the signal is measured without the predivider if the frequency is below 400 MHz, otherwise the divider remains connected.

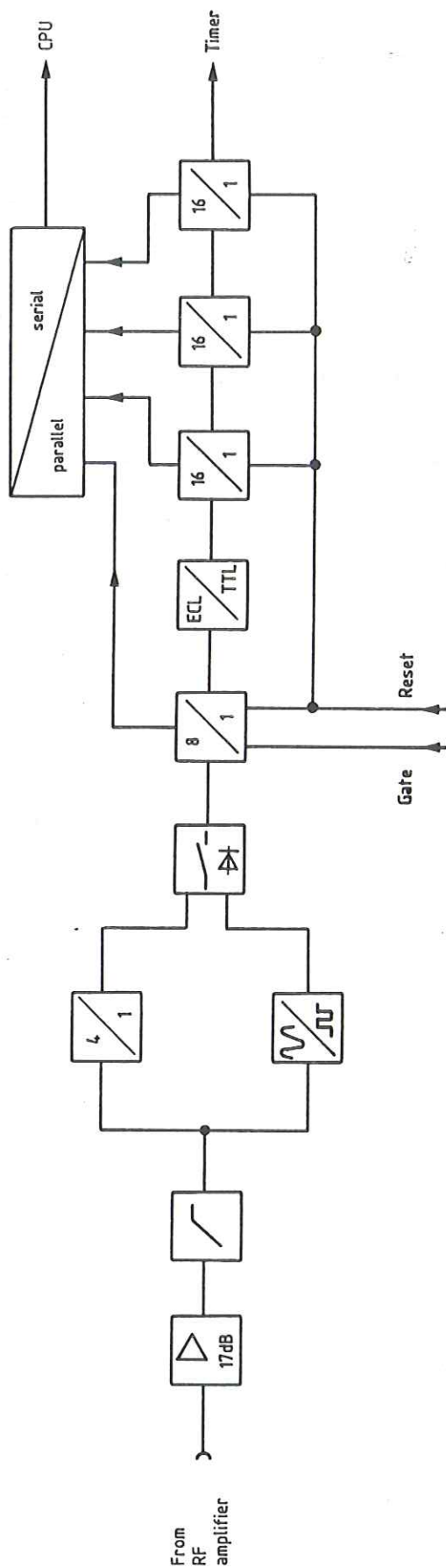


Fig. 5-4 Block diagram of the RF counter

5.1.14 AF Counter

The AF counter counts frequencies in the range from 10 Hz to 500 kHz. The signal to be counted is first amplified and then applied to two comparators. The reference signal of the comparators is then obtained from the positive and negative peak values of the counted signal. The output signals are applied to a clock-edge-controlled flip-flop with reset and then processed further in a special timer chip.

The advantage of this comparator control by a reference signal which depends on the amplitude of the input signal is the excellent processing even of noisy signals, as shown in Figs. 5-5 to 5-7.

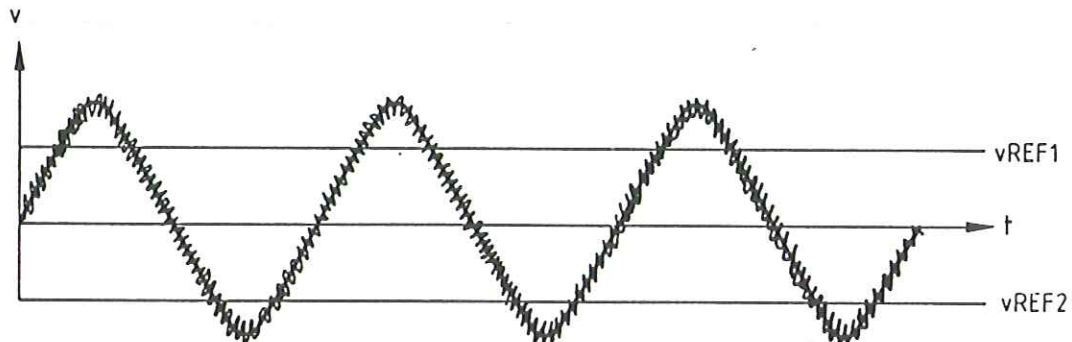


Fig. 5-5 Noisy input signal of comparators with reference voltage indicated

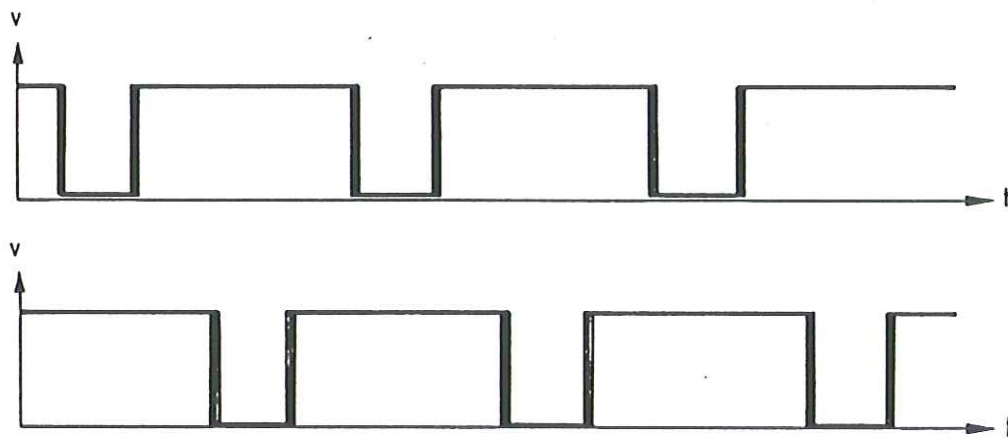


Fig. 5-6 Output signal of comparators with phase jitter

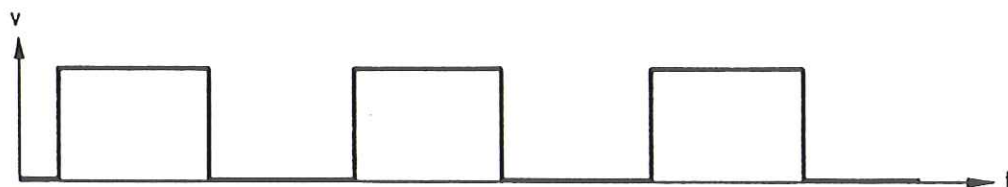


Fig. 5-7 Output signal of the flip-flop without phase jitter

5.2 Testing and Adjustment

5.2.1 Testing the A/D Converter Unit

The signal ground (SIGGND) must be connected to the main ground (GND). The plug-in jumper X75 must be inserted when operating the digital unit.

5.2.1.1 Reference Source

Measure the reference voltage against the signal ground (X1.A,B31) at test point P12 using a voltmeter. The voltage should be +10.000 V $\pm$ 1 mV and can be adjusted if necessary using R109.

5.2.1.2 A/D Converter

Measure the DC voltage at test point P11 after testing and adjusting the reference source. It should be -100 mV $\pm$ 5 mV compared to the signal ground. Apply a binary data word (X value) to the input of the D/A converter N100.

Apply a test voltage V_t to the signal input (MESSDC) (plug X1.A31 and test point P10) referred to the signal ground SIGGND (plug X1.A,B30). Vary the test voltage V_t such that the voltage range (see following table) associated with the X value is passed through.

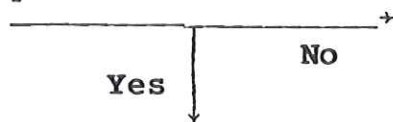
The TTL level at pin 7 of comparator N102 must change from High to Low if V_t is changed to higher values. The comparator voltage V_t associated with the changeover point must be within the tolerance associated with the X value.

The following table lists examples for three different X values:

X value	Tolerance within which the comparator changes from High to Low	
	Lower limit	V_t Upper limit
0	-240 mV	-160 mV
512	+4.990 V	+5.290 V
1023	+10.190 V	+10.750 V

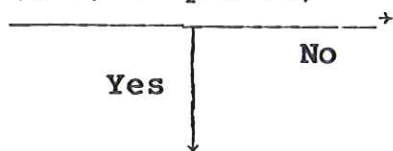
5.3 Troubleshooting

Are the supply voltages
+5 V and V_{BU}
present ?

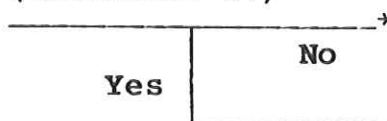


Test power pack and
leads.

Is the 5-MHz system
clock present ?
(CPU, D1 pin 56)

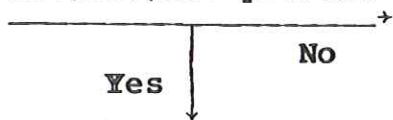


Is external 10-MHz
clock applied ?
(connector X7)



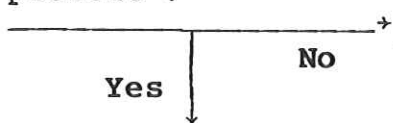
Check clock
source and
leads.

Check plug-in jumpers.
X20,X21,X27 present ?



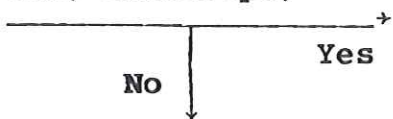
Insert plug-in jumpers.

Check power-fail
circuit. Signals
 V_{BU} , $CSRB$, RESET
present ?



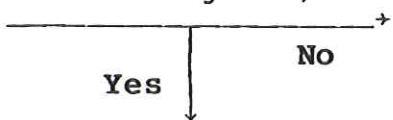
A

Are blocking CPU
signals at active
level ? (e.g.
DMA, interrupt)



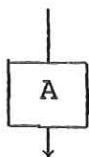
Eliminate level error
or check interrupt ex-
tension logic.

Are RAMs and EPROMs
correctly addressed ?
(addresses, data,
control signals)



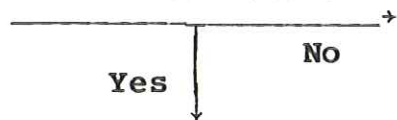
Check bus driver and
address decoder.

Continue trouble-
shooting with logic
analyzer, emulator,
oscilloscope.



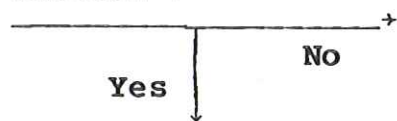
Power-fail circuit
faulty.

Is the signal
POWFAIL correct ?



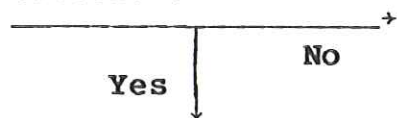
POWFAIL signal
line and power
pack.

Is the signal $\overline{\text{RES}}$
correct ?



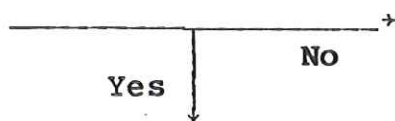
Check D47, D48 and
their circuitry.

Is the signal RESET
correct ?



Check $\overline{\text{RES}}$ and RESET
lines. Are both lines
OK ?

Change changeover
of RAM supply.
Check timing of
signal CSRB.



Eliminate
fault.

Check CPU (D1) and
replace if necessary.